REMARKS

Applicants kindly request that the examiner acknowledge Applicants' claim to foreign priority and receipt of the certified priority document in the next Office Action. Also, Applicants request that the Examiner acknowledge acceptance of the drawings.

Claims 1-10 are all the claims pending in the application. Claim 1 first stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner states that it is not clear how the scattered area information is used. While Applicants are not entirely sure, Applicants believe that the Examiner is referring to the "scattered areas" recited in the preamble of claim 1. Applicants submit that scattered areas, as know in the art, represent areas of starting and ending addresses specified by the area-specified vector scatter instruction. Applicants respectfully submit that the Examiner's misunderstanding of the use of vector scatter instructions (VSC) in association with scattered areas may be the basis for application of art (Kamiya) based on vector store instructions (VST), rather than VSC as described below.

Specifically, claims 1 and 2 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kamiya, U.S. Patent No. 5,247,635. Applicants respectfully traverse this rejection. As its title indicates, Kamiya is related to a vector processing system for invalidating scalar cache memory indicated by an address in a tentative scalar *store* instruction. On the other hand, the present invention, as recited in claims 1 and 2 is related to "controlling a vector *scatter* instruction." Applicants submit that Kamiya does not disclose or suggest use of vector scatter instructions (VSC). As Applicants provide in paragraph [0014] on page 4 of the present specification, a cache invalidation process differs between VST instruction, as disclosed in

Kamiya, and VSC instruction, as recited in the claims of the present invention. The differences are detailed in paragraphs [0015] through [0023]. As Applicants further provide in the present specification at paragraph [0024], it is an object of the present invention to improve performance of systems operable to use vector scatter instructions (VSC). Accordingly, since Kamiya does not disclose or suggest use of vector scatter instructions, Applicants submit that claims 1 and 2, as well as the remaining claims that recite the use of vector scatter instructions are allowable for this reason alone.

Further, discussing the rejection, the Examiner alleges that Kamiya teaches the invention of claims including a circuit for controlling a vector scatter instruction (citing col. 3, line 35). Applicants note that line 35 relates to a vector store instruction (VST) not a vector scatter instruction (VSC) as claimed. In addition, the Examiner states that Kamiya teaches means for detecting (citing col. 3, line 65) if an address to be accessed by the area specified vector scatter instruction overlaps with an address to be accessed by memory access instructions that follow the vector scatter instruction (citing col. 4, line 9). However, this section discusses a waiting process quite different from what is recited. That is, in present invention, the LDS instruction (memory access instruction) is issued after the VSC instruction. Notwithstanding the fact that Kamiya discusses VST instructions and not VSC instructions, the section that the Examiner cites indicates that the scalar load/store instruction that the Examiner alleges is the memory access instruction of Kamiya may issue before the vector store instruction (VST) ("the passing control unit 3 causes processing for the scalar load/store instruction to wait until a vector store instruction is issued from the instruction issuing unit 1 and processed."). Accordingly, the

Examiner has additionally not shown how this feature is anticipated by Kamiya in light of Kamiya's use of tentative issued vector store instructions.

Next, the Examiner states that the "means for holding the memory access instruction that follows the vector scatter instruction if the addresses overlap" is disclosed by col. 4, line 11. Again, like above, this section of Kamiya indicates that a scalar load/store instruction may be issued prior to the vector store instruction (as these instructions are equated to the present invention by the Examiner). Therefore, the Examiner has not shown how this feature is anticipated by Kamiya.

Claims 3-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kamiya. The Examiner states that Kamiya teaches the invention substantially as claimed as discussed above for claims 1 and 2, however, the Examiner acknowledges that Kamiya does not expressly state that the vector scatter instruction comprises a predetermined field specifying a starting address register and an ending address register and two comparators that are used to determine whether the memory access address falls within the range. Nonetheless, the Examiner argues that the reference teaches vector scatter instruction comprising a predetermined field specifying the start address and length of the range and teaches how to obtain the end address (citing col. 3, line 51).

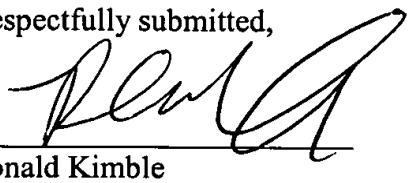
First, in this breif rejection of several claims, the Examiner fails to state how the claimed comparators are disclosed. In addition, Applicants respectfully submit that the Examiner's broad rejection is insufficient to establish that the features of claims 3-9 are disclosed or suggested by Kamiya. For example, the Examiner does not discuss or cite sections of Kamiya that show how

any of the recited structure is taught or suggested. This includes a plethora of features, such as a vector unit, a vector scatter address conflict detection unit, a vector scatter address coincidence detection unit, a circuit operable using vector scatter instructions, logical circuit, etc. Applicants note that MPEP 707.07(d) states that this type of "omnibus" rejection is to be avoided. Accordingly, the Examiner is respectfully requested to allow the claims based on their distinguishing features as discussed above, or issue a Non-Final Office Action that discusses the numerous allowable features recited in claims 3-9.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Ronald Kimble
Registration No. 44,186

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
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CUSTOMER NUMBER

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